

MULTI CHANNEL TIMING CHIP

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In many high energy physics experiments, a system is required to digitize the moment an event has occurred. These systems include various types of drift chambers and possibly all detector outputs in high rate none-clocked beam experiments. These experiments can lead to the requirement of tens of thousands of individual channels operating at extremely high rates. Most existing solutions [1] consist of custom chips for the front-end tied to a jungle of digital processing devices to get performances of about one nanosecond resolution. Many of these custom chips, implemented by various research centers and universities are designed at great labor cost and are only fleetingly available for a short few years until the experts that have designed them move on or the attending fabrication processes become no longer available. Almost all solutions suffer from significant dead time in a high rate environment. This proposal suggests a solution to overcome all these existing problems and deliver large systems with a time resolution of one nanosecond with no dead time and relatively short latency. Cost is still a major issue. At this time, there is a push to enlarge digital devices to accommodate high bandwidth signal paths in order to reduce the number of signal lines and match the speed performance of the interior logic. This is usually done by time multiplexing many signals sequentially onto a single line and transmitting that signal either through an optic fiber or through a differential wired path. Industry calls this SERDES (serialize, deserialize). A favorite and effective standard for these signals is the LVDS, low voltage differential signaling. Altera, a manufacturer of system size field programmable gate arrays (FPGA) is delivering chips with 36 input LVDS ports capable of operating at a bit serial rate of 1000MHZ. These devices receive and convert the data into selectable length parallel words. The output length should be of such a value as to allow the interior logic elements to operate at reasonable frequencies. This must be over 250MHZ. This document describes a current design effort to create such a device with the plan of initially building a sample demonstration board.

1 The Overall Design

The device for which this project is targeted is the Altera EP2A15, the smallest of the APEX II family [2]. Features of this chip are thirty-six LVDS inputs that can capture data at one gigahertz driven by two separate clocks. They are internally clocked from phase locked loops operating at eight times the rate of an external one hundred twenty five megahertz reference. There are typically 600,000 gates and 104 blocks of 4 kilobits of memory. These resources are necessary for logic elements and temporary storage to enable the no dead time feature. The serial data is programmed to transfer

eight sequential one-nanosecond interval bits into a single eight-bit word every eight-nanosecond period. These bytes are concatenated in a shift register to present two sequential bytes to a "runt filter". The purpose of this filter is to assure that a transition from low to high or high to low, exists for at least four nanoseconds. Since each bit represents one nanosecond, a simple filter made of a parallel logic array is designed to operate in the eight-nanosecond interval. It is possible to detect two valid transitions in the eight-bit interval. Since the specification require that the device be without dead time, the resulting tagged filtered data containing a transition, is transferred into a 32 word FIFO as new data enters the filter. The entire front end of this chip, from LVDS input to FIFO input, is synchronous. The only other portion of this design that must operate synchronously with the input clock is a single eight-bit counter, which counts once every input clock tick to produce the coarse time data. This is loaded with the fast data image creating the total time image with a resolution of one nanosecond in over a 2-microsecond interval. Transitions can occur with as little as four nanoseconds spacing. The proposed limit per channel is 32 transitions, the size of the channel FIFO. Other features of the chip are two bits in each channel to indicate an event number. The channel's FIFO are scanned into a chip FIFO for later presentation to the collecting processor. The scan may or may not be limited by the event number or all recorded data can be collected. This scan can be done at a relaxed rate since in most applications the total number of valid hits will be only a small portion of the chip capacity.

2 The Serial to Parallel Converter

This new feature, implemented into the ALTERA Apex II device family, contributes strongly to the possibility of designing this chip. This device accepts differential inputs at frequency as high as one gigahertz and can form parallel words from this stream. The data must be clocked from a dedicated phase lock loop, which supplies a clock equal to the input data rate. This is a programmable value. The same loop also can generate a second synchronous clock that is a portion of the input rate to drive the interior logic of the chip. Figure 1 shows the bit position within the serial train. The output of this converter is collected in the first of two eight-bit shift register stages for presentation to a runt filter.

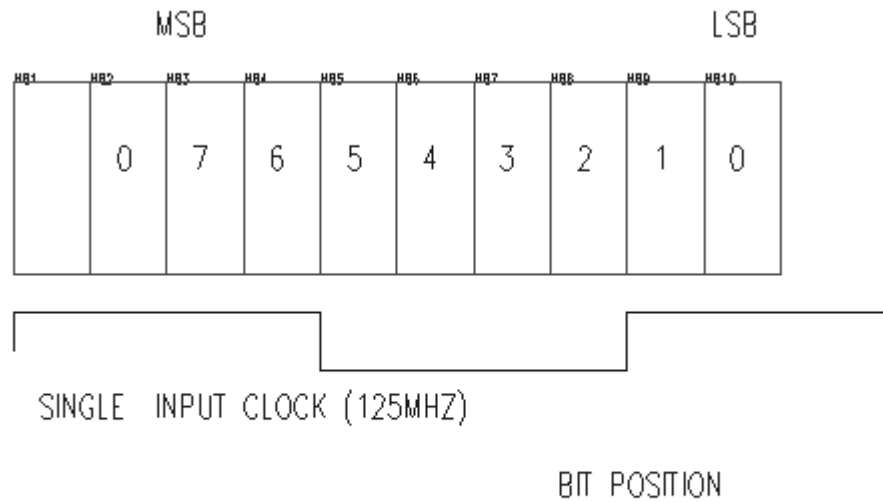


Figure 1. Serial train.

3 A Single Channel

The output parallel byte is shifted into second register so that the prompt and late bytes may be presented at once to a runt filter. The results of the runt filter are stored in another register together with global coarse time value and an event number identifier. The results of this entire block are then passed to a channel FIFO. This is all shown in Figure 2.

4 The Runt Filter

This device scans the input stream to search for transitions that will cause a level domain that exists for at least four nanoseconds. This prevents false sightings due to input noise and will minimize the normal traffic. Two bytes are concatenated to present eight bits that span the transition between the sequential bytes. Essentially, the filter is an array of gates, each having six inputs. One input represents the initial state and four other inputs are the states of the four following time intervals. The final input is the existing

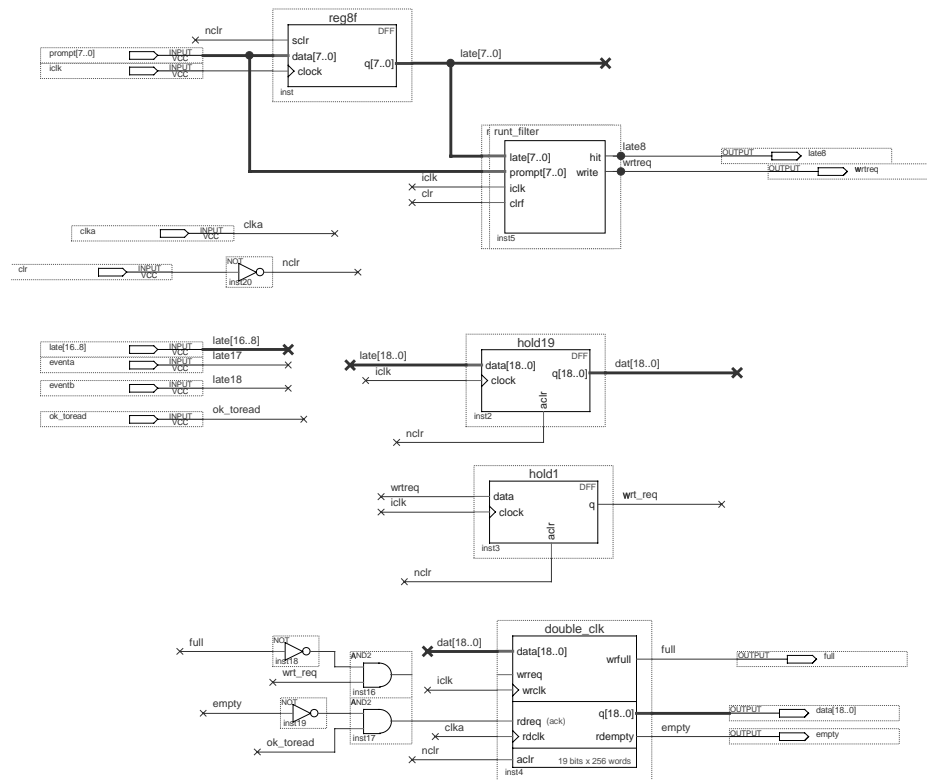


Figure 2. Single input channel.

state of the line. A gate is included for each unique time position and for either transition direction. It is possible to have two transition in the period presented to the filter. When that possibility arises a signal, "hit", the state of the input, is latched or cleared and is then subsequently included in the final filter stage. This logic must perform both half clock period decisions in eight nanoseconds before the input stream is updated. The output is the

"hit" bit and the second stage of the shift register, "late [7..0]"

5 Detail of the Top Design

The software supplied by Altera for compiling this chip, allows for such simple hierarchy design strategies. Copying the single channel symbol 18 times essentially created this design. This design has been successfully compiled and simulated to show that the input stream can operate with one nanosecond interval resolution. The result of this compilation has shown that this design, at 50 percent of the target goal has used only 16 percent of the chip logic elements and 20 percent of the included memory. The time simulation had shown that all signal paths ran at the design speed without error.

6 Future Plans

We intend to finish the design of this FPGA to the maximum target of 36 input channels. We then plan to fabricate a circuit board that will include one of these chips for a useful capacity of 35 channels. One input will be dedicated to a common start or stop time. This allows a time differential measurement to be made with a resolution of one nanosecond. When this preliminary design succeeds, we will follow with a production size board with three of the subject chips allowing as many as 104 useful channels. The "Quartus" tools used for this design were supplied by the chip vendor, Altera Corporation. Complete data entry, compile and simulate modules are part of this package. Models for every logic function are supplied. We expect the price of this chip to decline as manufacturing yield improves and competition increases. For large volumes, this chip can be converted to a mask-programmed version to achieve considerable unit cost savings.

References

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