

Status and New Layout of the ATLAS Pixel Detector.

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on behalf of the ATLAS Pixel collaboration [1]

Abstract:

The ATLAS Pixel detector is based on a set of radiation-hard electronics chips able to resist a dose of 500kGy. The implementation of these chips in the DMILL technology did not give the expected results. Re-design of the radiation-hard chips in DeepSubMicron technology is ongoing, but has implied a one and a half year delay in an already tight schedule. Major layout changes have therefore been necessary to allow installation of the ATLAS pixel detector at LHC start-up.

This paper illustrates the status of the ATLAS pixel project, the motivations for the new layout, the way this should be implemented and the prototype fabrication and testing.

1. INTRODUCTION

The ATLAS Pixel detector has been already described elsewhere [1] and will be only briefly recalled here. This detector should be able to measure three space points in the pseudorapidity region up to $|\eta| = 2.5$. It is made of two barrel layers, initially having 10.1 cm and 13.2 cm radius, plus so called b-layer of 4.3 cm radius. The main aim of the b-layer is to allow better impact parameter resolution for B-physics and for b-tagging. The forward region is covered by set of 5+5 disks with internal and external radii of, respectively, 12.6 cm and 18.7 cm. The detector system is composed of modular units (fig.1). Each module consists of a silicon sensor tile, sixteen front-end readout integrated circuits (FE chips) and a kapton flex hybrid (fig.2). The flex hybrid distributes power and control signals to the FE chips and allows reading them out through a module control circuit (MCC). Passive components including termination resistors, decoupling capacitors and temperature sensor are also included. The sensitive area of a module, i.e. of a sensor tile, is 16.4 mm x 60.8 mm. The FE chips are connected to the pixel cells through bump bonds. The size of one pixel is 50 μm x 400 μm and each FE chip serves 18 x 160 pixel cells. The flex hybrid is glued to the backside of the sensor tile; electrical connections from the MCC and the 16 FE chips to the flex hybrid are done through ultrasonic wedge-bonding.

2. RADIATION HARDNESS

2.1 Sensors

Radiation damage in the severe LHC environment can result in a voltage for

full depletion of silicon detectors, which may exceed the maximum allowed operation voltage, and thus requires the detectors to be operated only in partial depletion [1]. The baseline design of ATLAS Pixel silicon sensors is characterized by:

- n^+ pixels on oxygenated n-bulk material (double-sided processing) to allow partially depleted operation [2],
- moderated p-spray isolation to allow for high voltage breakdown after the type inversion,
- a bias grid to allow the sensor testing before module assembly.

The sensors radiation hardness to 10 years of LHC operation has been proven [3]. One of the proofs recently obtained is the interpixel isolation test, which demonstrates no ionization-induced damage (fig.3). The sensors under test have been irradiated up to 500 kGy with 20 keV electrons; bias voltage of 500 V has been applied during the irradiation. The I-V curves show the pinch off at higher voltages for the irradiated sensor, but the interpixel isolation (about 100 MOhm at 100 V bias) is still sufficient.

The preproduction of 150 good tiles has been done; careful tests have confirmed that the ATLAS specifications are met. The production will start in January 2002.

2.2 Electronics

The four integrated circuits: FE chip (16 per module), MCC (event builder for 16 FE chips), VDC (VCSEL Driver Chip to drive data off-detector) and DORIC (to decode/encode clock and control signals) have been implemented in the DMILL radiation hard technology. Despite the large efforts of the Pixel collaboration this technology has not been able to

produce the most complex chips (FE and MCC) with acceptable yield. Therefore the DMILL design work was stopped and maximum priority had been given to translate the various designs to the DeepSubMicron (DSM) technology.

First digital DSM test chip had some limited functionality but worked roughly as expected. The analog test chip had been submitted to IBM and TSMC in February / March 2001. This chip contained the preliminary designs of analog blocks of 20 pixels and other analog circuits, as well as the final layout of the critical items. On-line results and first tests done after irradiation (at a dose of 610 kGy with 55 MeV protons) indicated little or no change in performance of the test chip (the reference current, one of the test chip important characteristics, is shown in fig.4.).

3. INSERTABLE LAYOUT

The failure of the DMILL design and the transition from DMILL to DSM has generated 1.5 years delay in the Pixel detector schedule and made impossible the “ready for installation” date initially foreseen (April 2004). This date was required to install the Pixel detector together with the Barrel Inner detector. The “Insertable” layout decouples the Pixel detector from the rest of the Inner detector and allows its independent installation later. This decoupling is obtained installing a 7 m long support tube together with the Barrel Inner detector. The Pixel system can then be slid in this support tube when the vacuum is broken and the forward section of beam pipe is out. The central section of beam pipe is integrated in the Pixel system and move with it. The Pixel

system, services and beam pipe are prepared on surface, lowered using a temporary support and rolled into the support tube held by SCT barrel. The services for all but b-layer should go out both sides. The b-layer services go out on one side to allow installation and dismantling together with the beam pipe in place.

To fit the SCT bore the Pixel system had to be squeezed (the outer barrel radius has been changed from 14.2 cm to 12.2 cm) and shortened (fig.5). The number of disks is reduced (from 5+5 to 3+3); all disks have been made equal (8 sector each) and come closer to the interaction point. The inner radius of the Pixel system has increased from 4.1 cm to 5.0 cm because of the beam pipe radius increase. In total, the detector active area is reduced by 17 %.

The Insertable layout has some reduced performance.

In the plot for probability to have less than 3 hits (fig.6) we see some losses due to clearances in the barrel section. The peak at $\eta = 1.5 \div 2.2$ is caused by inability of getting the first disk close enough to barrels, while the peak at $\eta = 2.5$ arise because the minimum inner radius of the disks must be compatible with the b-layer insertion.

The Pixel detector material is increased at high η and become more asymmetric since b-layer services exit one side (fig.7).

The impact parameter resolution (fig.8) degrades at low momenta due to the b-layer radius increase.

4. LOCAL SUPPORTS

It was necessary quite some ingenuity to preserve most of the mechanical design of ATLAS Pixel system already done, including both local supports: barrel staves and disk sectors. The shingled stave support (fig.9a) offers hermetic coverage over the full acceptance range of each barrel pixel layer. Pixel modules are glued onto the carbon-carbon thermal management tiles (TMTs) to form individual mechanical modules. The TMTs have a machined groove, which accommodates a cooling tube, and makes contact to it through thermal grease. In the disk part the Pixel modules are placed on both sides of each disk to ensure continuous active coverage. This placement leads naturally to a sandwich construction for the disks with facings of high stiffness and high thermal conductivity on either side of a light core with an embedded coolant channel. A disk is divided into the angular regions, called sectors (fig.9b), of convenient size and cooling load.

The set of quality control tests has been defined to estimate the local supports quality [4]. In order to achieve an acceptable lifetime of silicon detectors, the operating temperature must be maintained at or below 0°C. The temperature of the pixel silicon sensors is determined by the heat load generated by the electronics attached to the sensors, the leakage currents in the sensors, the heat flow from the surrounding power and cooling services and heat flow from/to outside the pixel detector volume. Since the heat transfer efficiency to the surrounding environmental gas is very low, the temperature of the sensors is driven by the heat dissipation efficiency of the

cooling structures. Therefore, the transverse thermo-conductivity of the local supports has to be measured. The carbon-carbon electrical resistance is used for the local support heating. The power applied to one stave shingle in the test is equal and simulates the typical power used by one detector module in operation. The cooling is being performed with turbulent water flux. The temperature control is done with a thermocamera. An example of a good stave thermo-image is shown on fig. 10a. The temperature structure on the image corresponds to the stave variable thickness and, therefore, the resistance. A stave internal structure defect has then been simulated: the thermal grease between the aluminium pipe and the carbon-carbon TMT has not been put for a length of ~1 cm. The temperature distribution along the defective stave (fig.10b) is significantly different from the regular one; the defect can be easily identified and the stave can be rejected at this early stage.

5. MODULE TESTS

The main quality factors of the pixel modules are: threshold and noise, both their mean values and their dispersion over the entire matrix, the number of dead pixels and the stability of all these values during the operation.

To check the operation and define the characteristics of each pixel module the following laboratory tests are performed:

- Digital test: digital signals are injected after each pixel discriminator; this allows to verify the proper functioning of the read-out chain.
- Analog test: analog signals are injected at each preamplifier input, this allows

to measure the threshold and noise values. After this test the tuning of threshold values for every FE chip is done.

- Test with source: ^{109}Cd (22KeV γ), ^{241}Am (60KeV γ), ^{90}Sr (β) are used to verify the whole chain (sensor-readout) quality. The self-triggering capability of the electronics greatly simplifies this kind of test.

About 20 functional pixel modules with slightly different electronics, flex and bump design have been assembled during the period 1998-2001. The threshold value at which it was possible to operate them varied between 3000e and 5000e, with sigma values of 150-300e. The noise value is in the range of 150e-300e. The typical threshold and noise distributions of the modules, which have been assembled recently, are shown in fig. 11.

The modules were operated on the SPS (H8, π^+ 180 GeV beam) at CERN, laboratory results have been confirmed including good stability.

6. CONCLUSIONS

A new Pixel detector layout that allows installation independent from the rest of the ATLAS Inner detector has been procured. This layout has minor acceptance and resolution losses, but facilitates installation, repair and upgrades. The mechanical changes did not offset the global schedule. The local

supports design did not need any change and their production will start soon. The sensors pre-production has been successfully completed. The laboratory and beam tests demonstrate the good performance and stable operational characteristics of pixel detector modules.

REFERENCES

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L. Rossi, The ATLAS pixel detector. Nuclear Instruments and Methods in Physics Research Section A 435 (1999) n.1, 2, pp 80-90.
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2. G. Lindstrom et al, Radiation hard silicon detectors-developments by the RD48 (ROSE) collaboration. Nuclear Instruments and Methods in Physics Research Section A, 466 (2001), n. 2, pp 308-326.
3. R. Wunstorff for the ATLAS Pixel collaboration, Radiation tolerant sensors for the ATLAS Pixel detector. Nuclear Instruments and Methods in Physics Research Section A, 466 (2001), n. 2, pp 327-334.
4. ATLAS Pixel Local Supports Requirements, ATLAS Project Document ATL-IP-EP-0005.

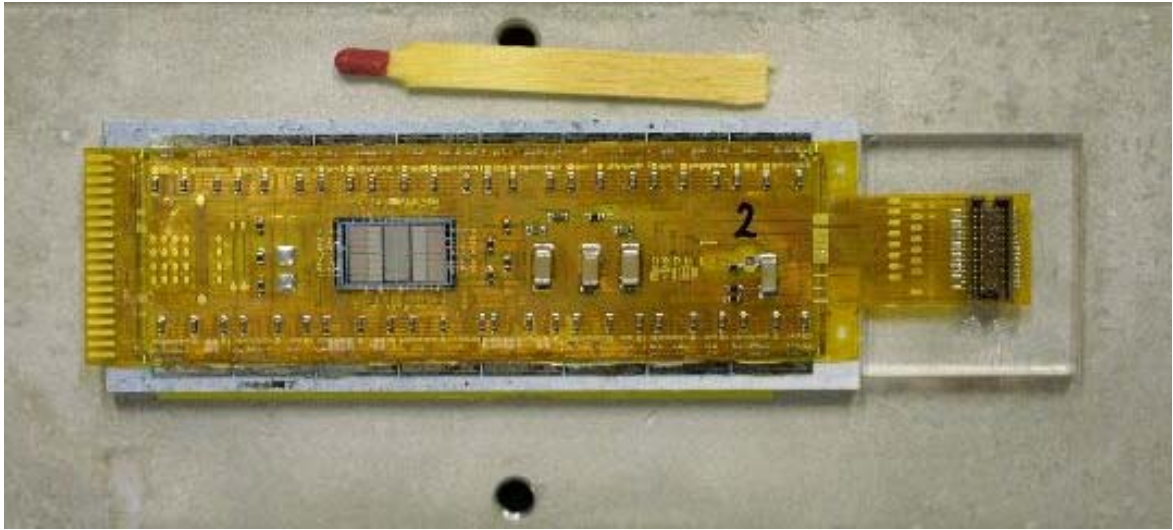


Fig.1. ATLAS Pixel module.

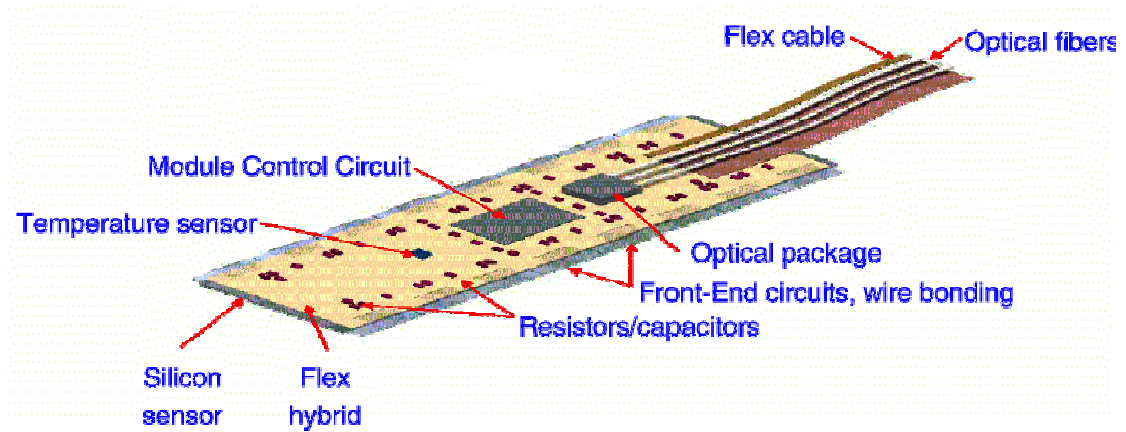


Fig.2. Module components.

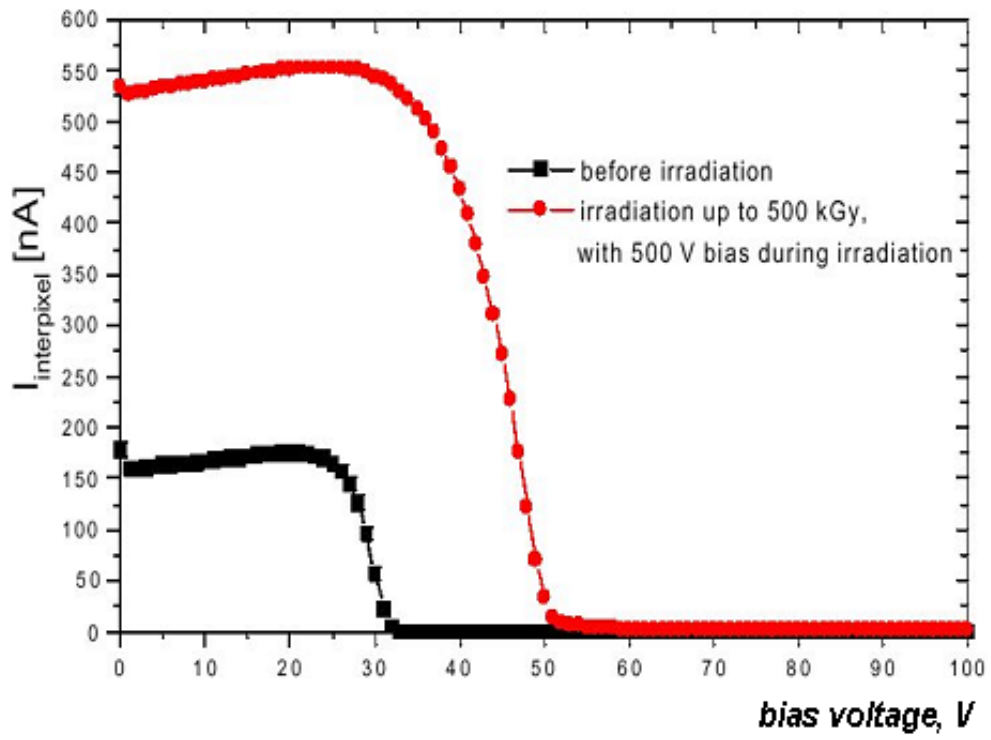


Fig.3. Interpixel isolation test (see text for details).

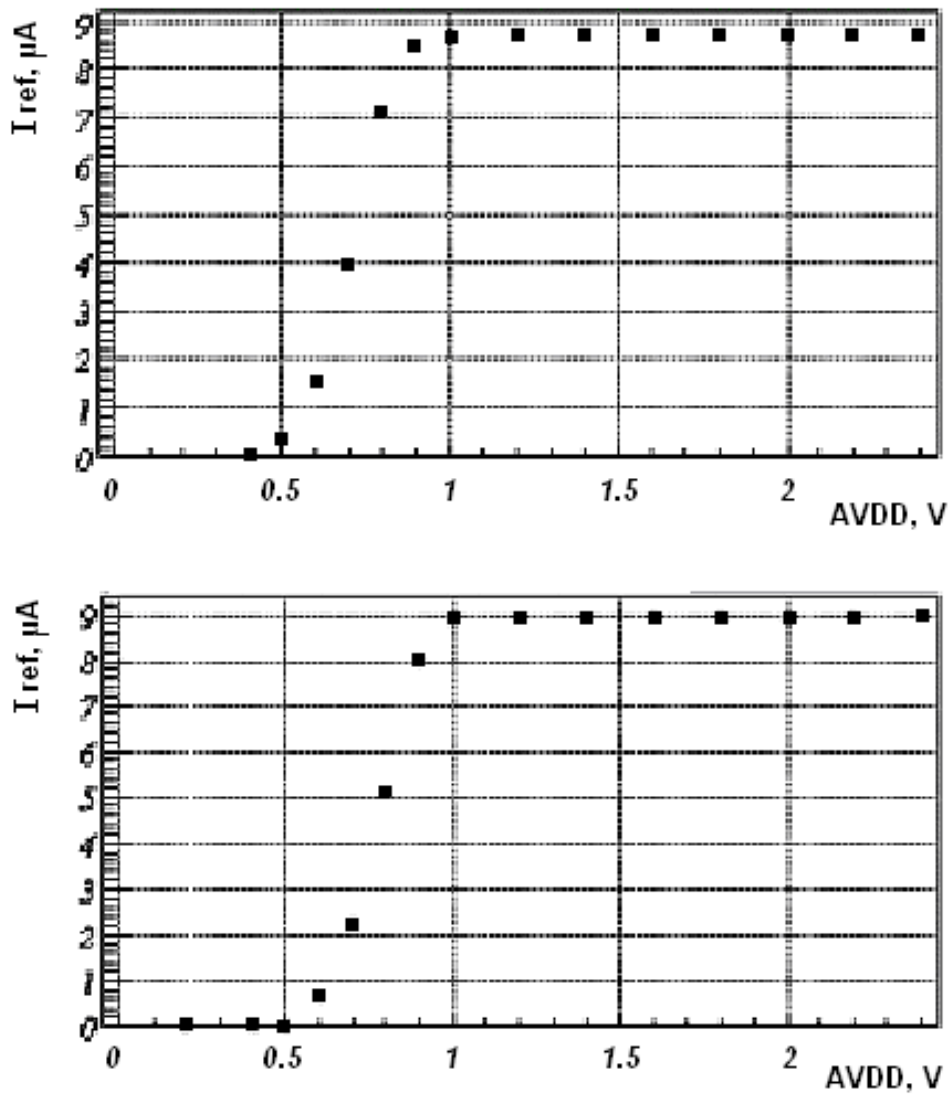


Fig.4. Analog test chip. Reference current versus analog voltage plot before (the upper plot) and after (the down plot) the irradiation of 610 kGy. A slight increase (~3%) in the plateau is observed.

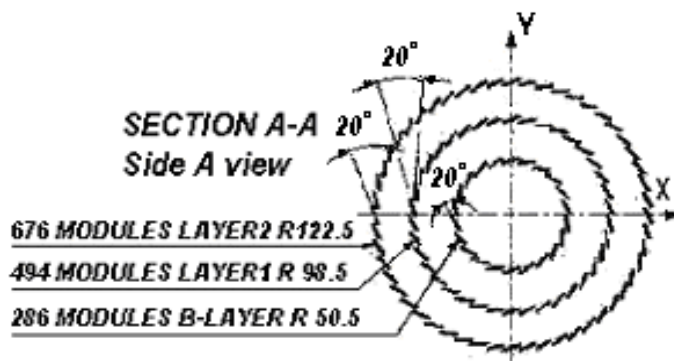
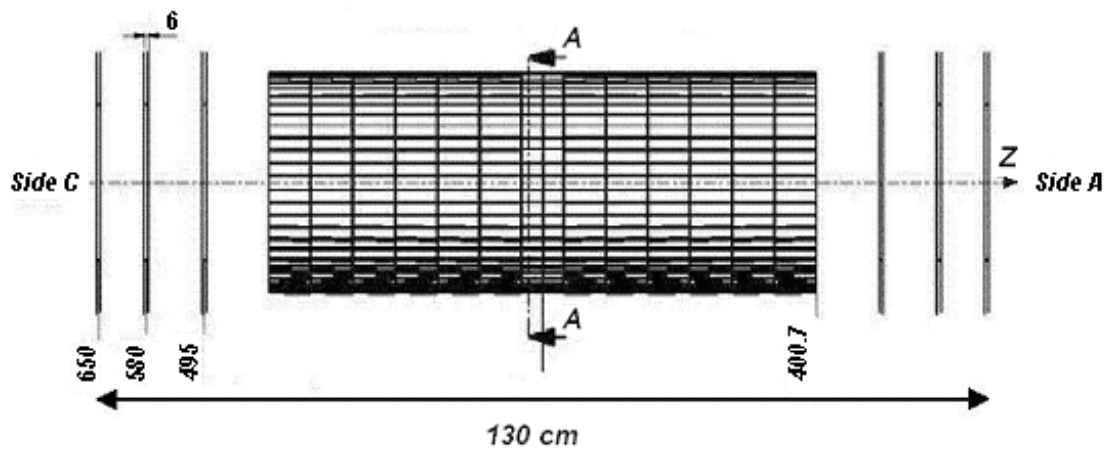


Fig.5. The new Pixel detector layout.

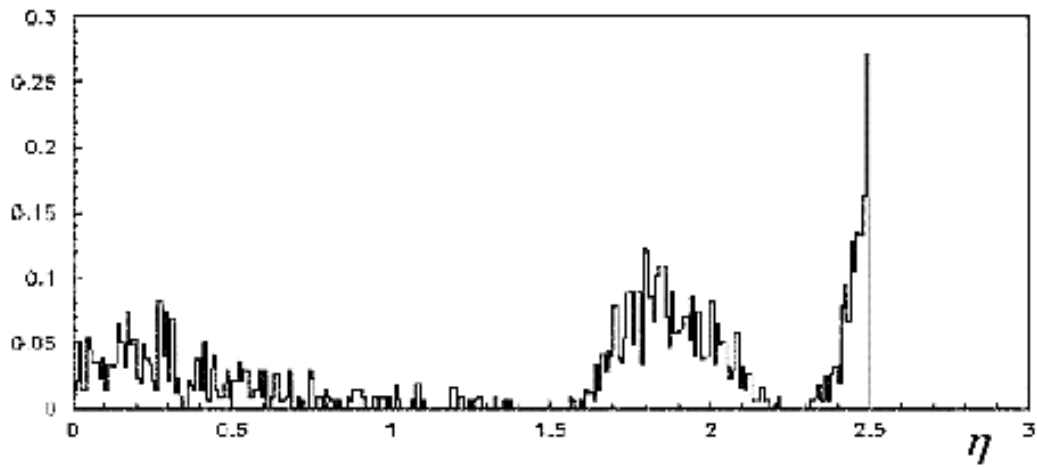


Fig.6. Probability for less than 3 layers hit versus pseudorapidity for the Insertable layout.

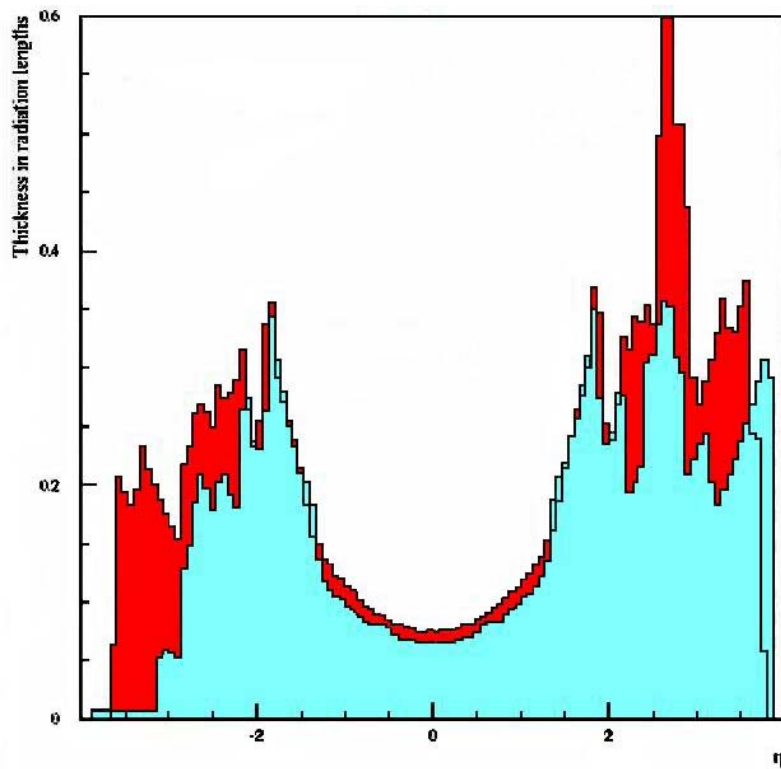


Fig.7. Material budget (X_0). Light: the previous layout, dark: Insertable layout.

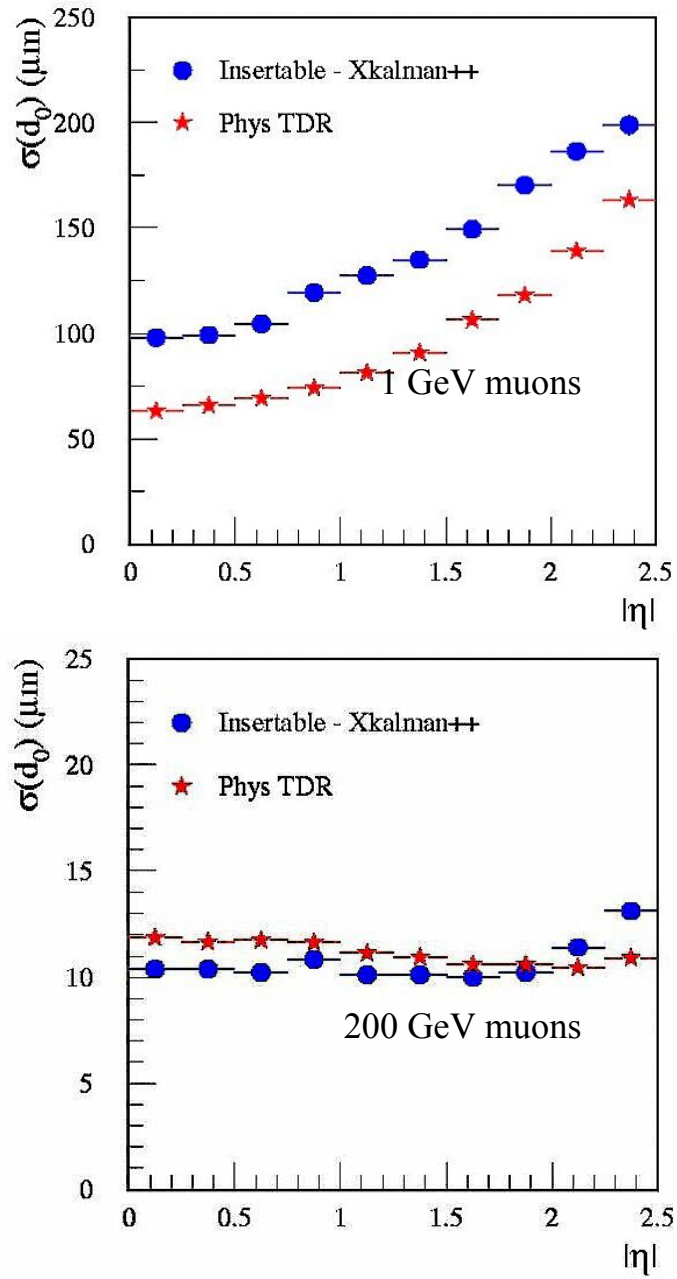
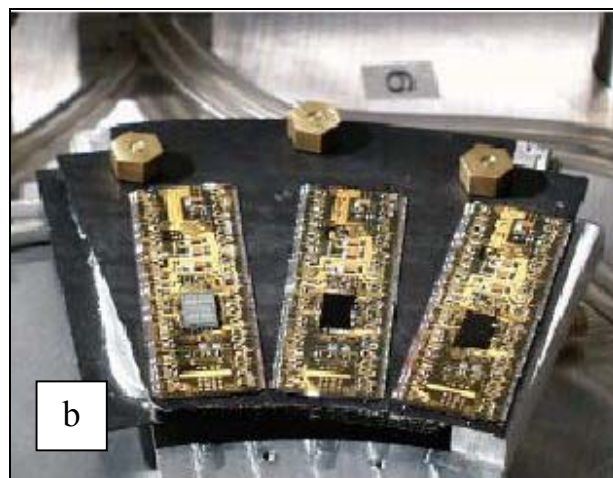


Fig.8. The impact parameter resolution for muons with different energy:
stars: Physics TDR, dots: Insertable layout simulation.



*Fig.9. Local supports: a) the bi-stave assembly: two staves with modules;
b) the sector assembly with modules attached on one side.*

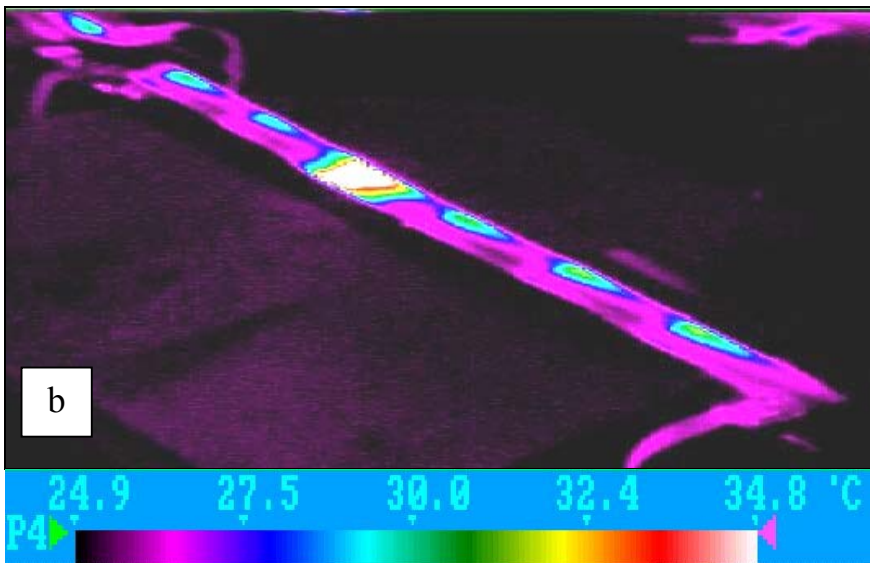
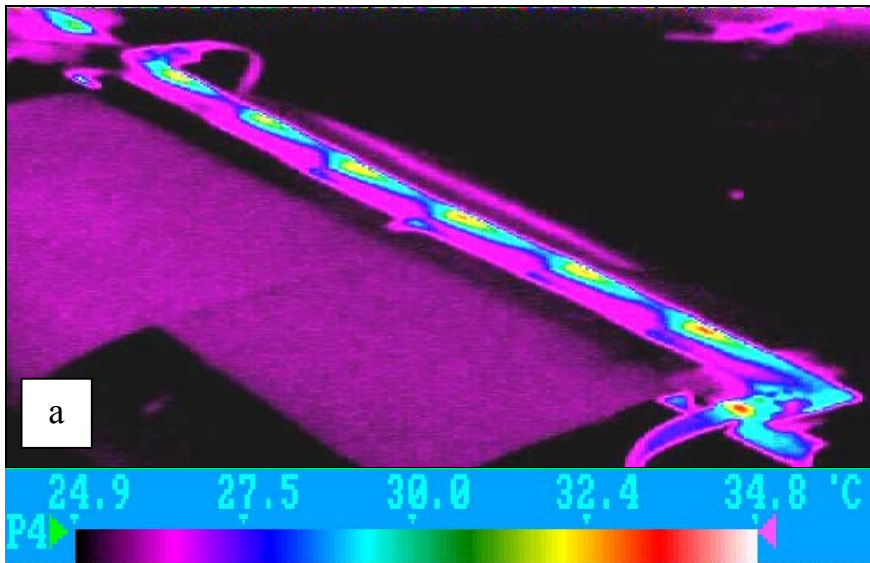


Fig.10. Local supports thermo-conductivity test: a) the good stave; b) the “defective” stave.

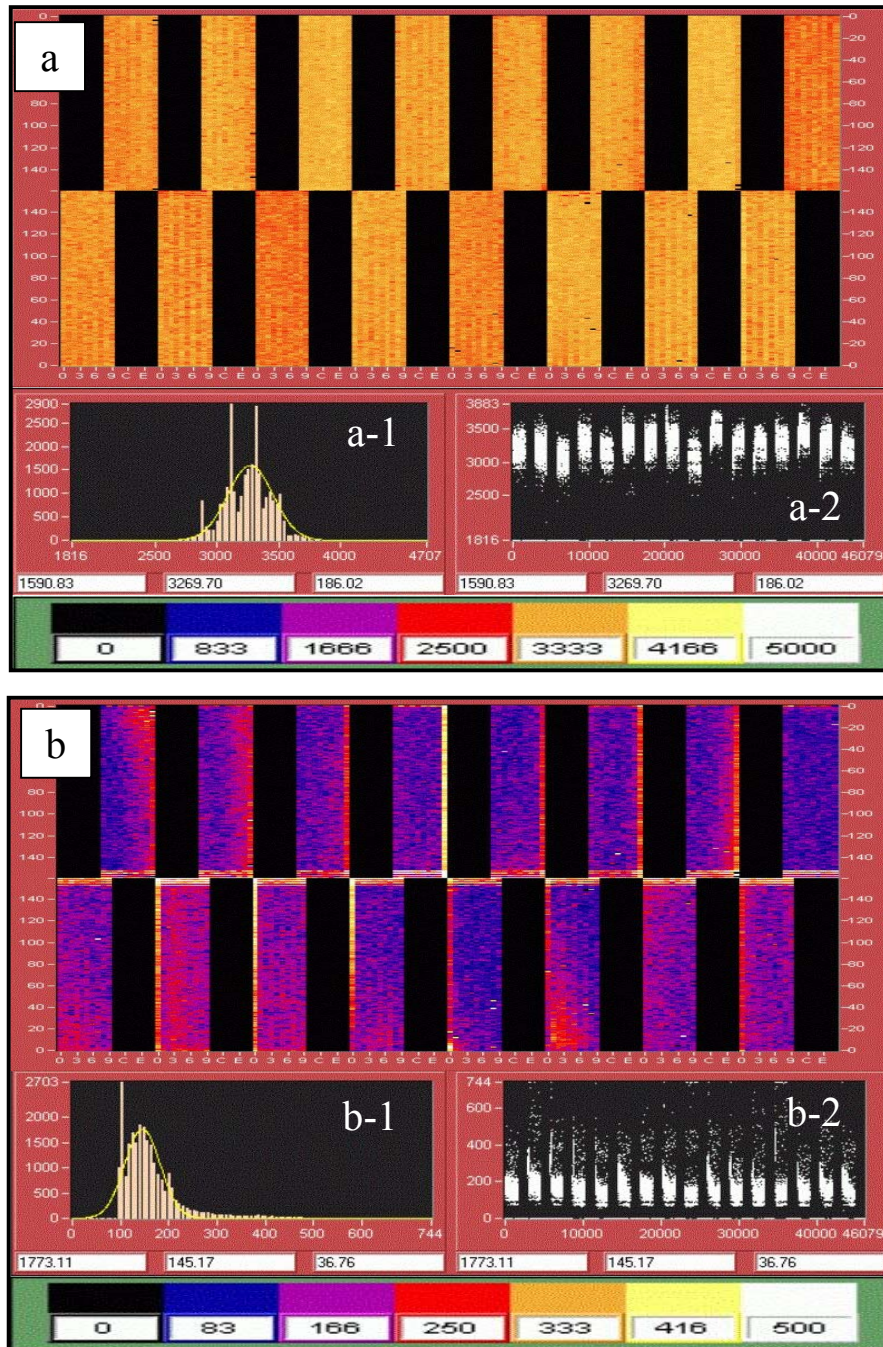


Fig.11. The typical threshold (a) and noise (b) maps of ATLAS Pixel modules. Threshold and noise values in e^- units are shown for every pixel (only 10 out of 18 columns of each FE chips are operational in this electronics design). In the windows a-1 and b-1 the threshold and noise plots for the whole module are shown. In the windows a-2 and b-2 the threshold and noise plots (value vs. channel number) are shown. Since there are missing channels corresponding to the columns 11-18, one may see the threshold and noise values grouped chip by chip on these plots.